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US 5598344 A	Method and system for creating, validating, and scaling structural description of electronic device	19970128	716/18
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, Nov.-Dec. 1998
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2 Author Index

Industry Applications, IEEE Transactions on , Volume: 34 , Issue: 6
, Nov.-Dec. 1998
Pages:1 - 42

[\[Abstract\]](#) [\[PDF Full-Text \(676 KB\)\]](#) **IEEE JNL**

3 Implementation of a state space controller in a FPGA

Garbergs, B.; Sohlberg, B.;
Electrotechnical Conference, 1998. MELECON 98., 9th Mediterranean
, Volume: 1 , 18-20 May 1998
Pages:566 - 569 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(256 KB\)\]](#) **IEEE CNF**

4 On-chip analog signal generation for mixed-signal built-in self-test

Dufort, B.; Roberts, G.W.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 3 , March 1999
Pages:318 - 330

[\[Abstract\]](#) [\[PDF Full-Text \(540 KB\)\]](#) IEEE JNL

5 Book Reviews

Circuits and Devices Magazine, IEEE , Volume: 16 , Issue: 6 , Nov. 2000
Pages:44 - 48

[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) IEEE JNL

6 Computer-aided design of analog and mixed-signal integrated circuits

Gielen, G.G.E.; Rutenbar, R.A.;
Proceedings of the IEEE , Volume: 88 , Issue: 12 , Dec. 2000
Pages:1825 - 1854

[\[Abstract\]](#) [\[PDF Full-Text \(552 KB\)\]](#) IEEE JNL

7 System specification experiments on a common benchmark

Gorla, G.; Moser, E.; Nebel, W.; Villar, E.;
Design & Test of Computers, IEEE , Volume: 17 , Issue: 3 , July-Sept. 2000
Pages:22 - 32

[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) IEEE JNL

8 FunState-an internal design representation for codesign

Strehl, K.; Thiele, L.; Gries, M.; Ziegenbein, D.; Ernst, R.; Teich, J.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 4 , Aug. 2001
Pages:524 - 544

[\[Abstract\]](#) [\[PDF Full-Text \(448 KB\)\]](#) IEEE JNL

9 The telecomputing laboratory: a multipurpose laboratory

DeBrunner, V.E.; DeBrunner, L.S.; Radhakrishnan, S.; Kamal Khan, A.;
Education, IEEE Transactions on , Volume: 44 , Issue: 4 , Nov. 2001
Pages:302 - 310

[\[Abstract\]](#) [\[PDF Full-Text \(65 KB\)\]](#) IEEE JNL

10 Modeling of mixed control and dataflow systems in MASCOT

Bjureus, P.; Jantsch, A.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 5 , Oct. 2001
Pages:690 - 703

[\[Abstract\]](#) [\[PDF Full-Text \(200 KB\)\]](#) IEEE JNL

11 A pipelined noise shaping coder for fractional-N frequency synthesis

Kozak, M.; Kale, I.;
Instrumentation and Measurement, IEEE Transactions on , Volume: 50 , Issue: 5 , Oct. 2001
Pages:1154 - 1161

[\[Abstract\]](#) [\[PDF Full-Text \(157 KB\)\]](#) IEEE JNL

12 Application of foresight's technology to implement a waveform development environment

Logan, B.; Wilson, D.;

Military Communications Conference, 2001. MILCOM 2001. Communications for Network-Centric Operations: Creating the Information Force. IEEE , Volume: 1 , 28-31 Oct. 2001

Pages:218 - 224 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(92 KB\)\]](#) IEEE CNF

13 Design of an optimized IC for control algorithms of AC machines: system testing and application

Fathallah, M.; Chante, J.P.; Calmon, F.; El-husseini, M.H.;

Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE , Volume: 1 , 30 Sept.-4 Oct. 2001

Pages:103 - 109 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(1312 KB\)\]](#) IEEE CNF

14 Practical considerations for a waveform development environment

Gudaitis, M.S.; Hinman, R.D.;

Military Communications Conference, 2001. MILCOM 2001. Communications for Network-Centric Operations: Creating the Information Force. IEEE , Volume: 1 , 28-31 Oct. 2001

Pages:190 - 194 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(142 KB\)\]](#) IEEE CNF

15 SPI - a system model for heterogeneously specified embedded systems

Ziegenbein, D.; Richter, K.; Ernst, R.; Thiele, L.; Teich, J.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 4 , Aug. 2002

Pages:379 - 389

[\[Abstract\]](#) [\[PDF Full-Text \(823 KB\)\]](#) IEEE JNL

16 Nanometer mixed-signal system-on-a-chip design

Chou, E.; Sheu, B.;

Circuits and Devices Magazine, IEEE , Volume: 18 , Issue: 4 , July 2002

Pages:7 - 17

[\[Abstract\]](#) [\[PDF Full-Text \(491 KB\)\]](#) IEEE JNL

17 Theoretical analysis of bus-invert coding

Rung-Bin Lin; Chi-Ming Tsai;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 6 , Dec. 2002

Pages:929 - 934

[\[Abstract\]](#) [\[PDF Full-Text \(367 KB\)\]](#) IEEE JNL

18 A methodology for system-level synthesis of mixed-signal applications

Oehler, P.; Grimm, C.; Waldschmidt, K.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume:

10 , Issue: 6 , Dec. 2002
Pages:935 - 942

[\[Abstract\]](#) [\[PDF Full-Text \(598 KB\)\]](#) IEEE JNL

19 Virtual benchmarking and model continuity in prototyping embedded multiprocessor signal processing systems

Janka, R.S.; Wills, L.M.; Baumstark, L.B., Jr.;

Software Engineering, IEEE Transactions on , Volume: 28 , Issue: 9 , Sept. 2002

Pages:832 - 846

[\[Abstract\]](#) [\[PDF Full-Text \(1097 KB\)\]](#) IEEE JNL

20 A design environment for high-throughput low-power dedicated signal processing systems

Davis, W.R.; Zhang, N.; Camera, K.; Markovic, D.; Smilkstein, T.; Ammer, M.J.; Yeo, E.; Augsburger, S.; Nikolic, B.; Brodersen, R.W.;

Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 3 , March 2002

Pages:420 - 431

[\[Abstract\]](#) [\[PDF Full-Text \(217 KB\)\]](#) IEEE JNL

21 Lorenz chaotic model using Filed Programmable Gate Array (FPGA)

Aseeri, M.A.; Sobhy, M.I.; Lee, P.;

Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 1 , 4-7 Aug. 2002

Pages:I - 527-30 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(298 KB\)\]](#) IEEE CNF

22 A component architecture for FPGA-based, DSP system design

Spivey, G.; Bhattacharyya, S.S.; Nakajima, K.;

Application-Specific Systems, Architectures and Processors, 2002.

Proceedings. The IEEE International Conference on , 17-19 July 2002

Pages:41 - 51

[\[Abstract\]](#) [\[PDF Full-Text \(371 KB\)\]](#) IEEE CNF

23 Customising floating-point designs

Gaffar, A.A.; Luk, W.; Cheung, P.Y.K.; Shirazi, N.;

Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on , 22-24 April 2002

Pages:315 - 317

[\[Abstract\]](#) [\[PDF Full-Text \(545 KB\)\]](#) IEEE CNF

24 On two new trends in evolvable hardware: employment of HDL-based structuring, and design of multi-functional circuits

Stoica, A.; Zebulum, R.S.; Keymeulen, D.; Ferguson, M.I.; Xin Guo;

Evolvable Hardware, 2002. Proceedings. NASA/DoD Conference on , 15-18 July 2002

Pages:56 - 59

[\[Abstract\]](#) [\[PDF Full-Text \(361 KB\)\]](#) IEEE CNF

25 From system specification to layout: seamless top-down design methods for analog and mixed-signal applications

Sommer, R.; Rugen-Herzig, I.; Hennig, E.; Gatti, U.; Malcovati, P.; Maloberti, F.; Einwich, K.; Clauss, C.; Schwarz, P.; Noessing, G.;

Design, Automation and Test in Europe Conference and Exhibition, 2002.

Proceedings , 4-8 March 2002

Pages:884 - 891

[\[Abstract\]](#) [\[PDF Full-Text \(632 KB\)\]](#) **IEEE CNF**

26 Implementation issues of neuro-fuzzy hardware: going toward HW/SW codesign

Reyneri, L.M.;

Neural Networks, IEEE Transactions on , Volume: 14 , Issue: 1 , Jan. 2003

Pages:176 - 194

[\[Abstract\]](#) [\[PDF Full-Text \(622 KB\)\]](#) **IEEE JNL**

27 Rapid prototyping of digital controls for power electronics

Monti, A.; Santi, E.; Dougal, R.A.; Riva, M.;

Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 3 , May 2003

Pages:915 - 923

[\[Abstract\]](#) [\[PDF Full-Text \(538 KB\)\]](#) **IEEE JNL**

28 Wordlength optimization for linear digital signal processing

Constantinides, G.A.; Cheung, P.Y.K.; Luk, W.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 10 , Oct. 2003

Pages:1432 - 1442

[\[Abstract\]](#) [\[PDF Full-Text \(650 KB\)\]](#) **IEEE JNL**

29 Design and testing of spacecraft power systems using VTB

Zhenhua Jiang; Shengyi Liu; Dougal, R.A.;

Aerospace and Electronic Systems, IEEE Transactions on , Volume: 39 , Issue: 3 , July 2003

Pages:976 - 989

[\[Abstract\]](#) [\[PDF Full-Text \(1984 KB\)\]](#) **IEEE JNL**

30 The synchronous languages 12 years later

Benveniste, A.; Caspi, P.; Edwards, S.A.; Halbwachs, N.; Le Guernic, P.; de Simone, R.;

Proceedings of the IEEE , Volume: 91 , Issue: 1 , Jan. 2003

Pages:64 - 83

[\[Abstract\]](#) [\[PDF Full-Text \(551 KB\)\]](#) [\[Full-Text HTML\]](#) **IEEE JNL**

31 Taming heterogeneity - the Ptolemy approach

Eker, J.; Janneck, J.W.; Lee, E.A.; Jie Liu; Xiaojun Liu; Ludvig, J.;

Neuendorffer, S.; Sachs, S.; Yuhong Xiong;

Proceedings of the IEEE , Volume: 91 , Issue: 1 , Jan. 2003

Pages:127 - 144

[\[Abstract\]](#) [\[PDF Full-Text \(976 KB\)\]](#) [\[Full-Text HTML\]](#) [IEEE JNL](#)

32 Design of optimal and narrow-band Laguerre filters for sigma-delta demodulators

Abeysekera, S.S.; Yao Xue; Charoensak, C.;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 50 , Issue: 7 , July 2003
Pages:368 - 375

[\[Abstract\]](#) [\[PDF Full-Text \(571 KB\)\]](#) [IEEE JNL](#)

33 Concurrent and simple digital controller of an AC/DC converter with power factor correction based on an FPGA

de Castro, A.; Zumel, P.; Garcia, O.; Riesgo, T.; Uceda, J.;

Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 2003
Pages:334 - 343

[\[Abstract\]](#) [\[PDF Full-Text \(926 KB\)\]](#) [IEEE JNL](#)

34 System level specification in Lava

Singh, S.;

Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003
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[\[Abstract\]](#) [\[PDF Full-Text \(KB\)\]](#) [IEEE CNF](#)

35 Perturbation analysis for word-length optimization

Constantinides, G.A.;

Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003
Pages:81 - 90

[\[Abstract\]](#) [\[PDF Full-Text \(334 KB\)\]](#) [IEEE CNF](#)

36 SystemC-AMS requirements, design objectives and rationale

Vachoux, A.; Grimm, C.; Einwich, K.;

Design, Automation and Test in Europe Conference and Exhibition, 2003 , 2003
Pages:388 - 393

[\[Abstract\]](#) [\[PDF Full-Text \(KB\)\]](#) [IEEE CNF](#)

37 Future design tools for platform FPGAs

Lysaght, P.;

Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on , 8-11 Sept. 2003
Pages:275 - 280

[\[Abstract\]](#) [\[PDF Full-Text \(279 KB\)\]](#) [IEEE CNF](#)

38 Accelerating bit error rate testing using a system level design tool

Singh, V.; Root, A.; Hemphill, E.; Shirazi, N.; Hwang, J.;

Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on , 9-11 April 2003

Pages:62 - 68

[\[Abstract\]](#) [\[PDF Full-Text \(342 KB\)\]](#) [IEEE CNF](#)

39 The EUROPRACTICE mini@sic program

Das, C.; McLean, J.;

Microelectronic Systems Education, 2003. Proceedings. 2003 IEEE International Conference on , 1-2 June 2003

Pages:45 - 46

[\[Abstract\]](#) [\[PDF Full-Text \(211 KB\)\]](#) [IEEE CNF](#)

40 Logarithmic arithmetic for real data types and support for Matlab/Simulink based rapid-FPGA-prototyping

Pohl, Z.; Schier, J.; Licko, M.; Hermanek, A.; Tichy, M.; Matousek, R.; Kadlec, J.;

Parallel and Distributed Processing Symposium, 2003. Proceedings. International , 22-26 April 2003

Pages:6 pp.

[\[Abstract\]](#) [\[PDF Full-Text \(423 KB\)\]](#) [IEEE CNF](#)

41 A middleware for signal-flow digital simulation models in electric vehicle powertrain

Cai Yunpeng; Sun Xiaomin; Jia Peifa;

Vehicular Technology Conference, 2003. VTC 2003-Fall. 2003 IEEE 58th , Volume: 5 , 6-9 Oct. 2003

Pages:3267 - 3271

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) [IEEE CNF](#)

42 An efficient methodology and semi-automated flow for design and validation of complex digital signal processing ASICS macro-cells

Tambour, L.; Zergainoh, N.; Urard, P.; Michel, H.; Jerraya, A.A.;

Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on , 9-11 June 2003

Pages:56 - 63

[\[Abstract\]](#) [\[PDF Full-Text \(357 KB\)\]](#) [IEEE CNF](#)

43 Rapid design and analysis of communication systems using the BEE hardware emulation environment

Chen Chang; Kuusilinna, K.; Richards, B.; Chen, A.; Chan, N.; Brodersen, R.W.; Nikolic, B.;

Rapid Systems Prototyping, 2003. Proceedings. 14th IEEE International Workshop on , 9-11 June 2003

Pages:148 - 154

[\[Abstract\]](#) [\[PDF Full-Text \(469 KB\)\]](#) [IEEE CNF](#)

44 An analytical integration method for the simulation of continuous-time /spl Delta//spl Sigma/ modulators

Gielen, G.G.E.; Francken, K.; Martens, E.; Vogels, M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 23 , Issue: 3 , March 2004

Pages:389 - 399

[\[Abstract\]](#) [\[PDF Full-Text \(568 KB\)\]](#) IEEE JNL

45 Multiparadigm Modeling in Embedded Systems Design

Muller-Glaser, K.D.; Frick, G.; Sax, E.; Kuhl, M.;

Control Systems Technology, IEEE Transactions on , Volume: 12 , Issue: 2 , March 2004

Pages:279 - 292

[\[Abstract\]](#) [\[PDF Full-Text \(1032 KB\)\]](#) IEEE JNL

46 Computer-Automated Multiparadigm Modeling in Control Systems Technology

Mosterman, P.J.; Sztipanovits, J.; Engell, S.;

Control Systems Technology, IEEE Transactions on , Volume: 12 , Issue: 2 , March 2004

Pages:223 - 234

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) IEEE JNL

47 Design and behavioral modeling tools for optical network-on-chip

Briere, M.; Carrel, L.; Michalke, T.; Mieyeville, F.; O'Connor, I.; Gaffiot, F.;

Design, Automation and Test in Europe Conference and Exhibition, 2004.

Proceedings , Volume: 1 , 16-20 Feb. 2004

Pages:738 - 739

[\[Abstract\]](#) [\[PDF Full-Text \(211 KB\)\]](#) IEEE CNF

48 Design, Automation and Test in Europe Conference and Exhibition Table of Contents

Design, Automation and Test in Europe Conference and Exhibition, 2004.

Proceedings , Volume: 3 , 16-20 Feb. 2004

Pages:v - ix

[\[PDF Full-Text \(184 KB\)\]](#) IEEE CNF

49 A framework for low power audio design

Vs, N.; Mertsching, B.;

VLSI Design, 2004. Proceedings. 17th International Conference on , 5-9 Jan.. 2004

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[\[Abstract\]](#) [\[PDF Full-Text \(274 KB\)\]](#) IEEE CNF

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1 Integrated Electronics for a Reading Aid for the Blind

Brugler, J.S.; Meindl, J.D.; Plummer, J.D.; Salisbury, P.J.; Young, W.T.;
Solid-State Circuits, IEEE Journal of , Volume: 4 , Issue: 6 , Dec 1969
Pages:304 - 312

[\[Abstract\]](#) [\[PDF Full-Text \(1792 KB\)\]](#) **IEEE JNL**

2 Design of embedded systems: formal models, validation, and synthesis

Edwards, S.; Lavagno, L.; Lee, E.A.; Sangiovanni-Vincentelli, A.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:366 - 390

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) **IEEE JNL**

3 Specification and analysis of timing constraints for embedded systems

Gupta, R.K.; De Micheli, G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 3 , March 1997
Pages:240 - 256

[\[Abstract\]](#) [\[PDF Full-Text \(536 KB\)\]](#) **IEEE JNL**

4 Embedded software in real-time signal processing systems: application and architecture trends

Paulin, P.G.; Liem, C.; Cornero, M.; Nacabal, F.; Goossens, G.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:419 - 435

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) [IEEE JNL](#)

5 Integrated circuit testing for quality assurance in manufacturing: history, current status, and future trends

Grochowski, A.; Bhattacharya, D.; Viswanathan, T.R.; Laker, K.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 44 , Issue: 8 , Aug. 1997
Pages:610 - 633

[\[Abstract\]](#) [\[PDF Full-Text \(468 KB\)\]](#) [IEEE JNL](#)

6 Hardware/software co-design of digital telecommunication systems

Bolsens, I.; De Man, H.J.; Lin, B.; Van Rompaey, K.; Vercauteren, S.; Verkest, D.;
Proceedings of the IEEE , Volume: 85 , Issue: 3 , March 1997
Pages:391 - 418

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#) [IEEE JNL](#)

7 A PAL/NTSC digital video encoder on 0.6- μ m CMOS with 66 dB typical SNR, 0.4% differential gain, and 0.2° differential phase

Cummins, T.; Murray, B.; Prendergast, C.;
Solid-State Circuits, IEEE Journal of , Volume: 32 , Issue: 7 , July 1997
Pages:1091 - 1100

[\[Abstract\]](#) [\[PDF Full-Text \(252 KB\)\]](#) [IEEE JNL](#)

8 1997 Index

Photonics Technology Letters, IEEE , Volume: 9 , Issue: 12 , Dec. 1997
Pages:0_5 - 0_92

[\[Abstract\]](#) [\[PDF Full-Text \(3884 KB\)\]](#) [IEEE JNL](#)

9 1997 Index IEEE Transactions On Applied Superconductivity Vol. 7

Applied Superconductivity, IEEE Transactions on , Volume: 7 , Issue: 4 , Dec. 1997
Pages:1 - 129

[\[Abstract\]](#) [\[PDF Full-Text \(5904 KB\)\]](#) [IEEE JNL](#)

10 The design of an adaptive on-line binary arithmetic-coding chip

Shiann-Rong Kuang; Jer-Min Jou; Yuh-Lin Chen;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 45 , Issue: 7 , July 1998
Pages:693 - 706

[\[Abstract\]](#) [\[PDF Full-Text \(424 KB\)\]](#) [IEEE JNL](#)

11 A 70-Mb/s variable-rate 1024-QAM cable receiver IC with integrated 10-b ADC and FEC decoder

Loke Kun Tan; Putnam, J.S.; Fang Lu; D'Luna, L.J.; Mueller, D.W.; Kindsfater, K.R.; Cameron, K.B.; Joshi, R.B.; Hawley, R.A.; Samueli, H.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 12 , Dec. 1998
Pages:2205 - 2218

[\[Abstract\]](#) [\[PDF Full-Text \(812 KB\)\]](#) [IEEE JNL](#)

12 A 3.3-V power adaptive 1244/622/155 Mbit/s transceiver for ATM, SONET/SDH

Belot, D.; Dugoujon, L.; Dedieu, S.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998
Pages:1047 - 1058

[\[Abstract\]](#) [\[PDF Full-Text \(368 KB\)\]](#) [IEEE JNL](#)

13 An agile ISM band frequency synthesizer with built-in GMSK data modulation

Filiol, N.M.; Riley, T.A.D.; Plett, C.; Copeland, M.A.;
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 7 , July 1998
Pages:998 - 1008

[\[Abstract\]](#) [\[PDF Full-Text \(220 KB\)\]](#) [IEEE JNL](#)

14 High-level power modeling, estimation, and optimization

Macii, E.; Pedram, M.; Somenzi, F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 , Issue: 11 , Nov. 1998
Pages:1061 - 1079

[\[Abstract\]](#) [\[PDF Full-Text \(300 KB\)\]](#) [IEEE JNL](#)

15 A cellular analog network for MRF-based video motion detection

Luthon, F.; Dragomirescu, D.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 46 , Issue: 2 , Feb. 1999
Pages:281 - 293

[\[Abstract\]](#) [\[PDF Full-Text \(840 KB\)\]](#) [IEEE JNL](#)

16 A real-time digital VCR encode/decode and MPEG-2 decode LSI implemented on a dual-issue RISC processor

Mohri, A.; Yamada, A.; Yoshida, Y.; Sato, H.; Takata, H.; Nakakimura, K.; Hashizume, M.; Shimotsuma, Y.; Tsuchihashi, K.;
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 7 , July 1999
Pages:992 - 1000

[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) [IEEE JNL](#)

17 Models for systematic design and verification of frequency synthesizers

De Smedt, B.; Gielen, G.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 10 , Oct. 1999
Pages:1301 - 1308

[\[Abstract\]](#) [\[PDF Full-Text \(140 KB\)\]](#) [IEEE JNL](#)

18 Pausable clocking-based heterogeneous systems

Yun, K.Y.; Dooply, A.E.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 7 , Issue: 4 , Dec. 1999

Pages:482 - 488

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) [IEEE JNL](#)

19 A 0.155-, 0.622-, and 2.488-Gb/s automatic bit-rate selecting clock and data recovery IC for bit-rate transparent SDH systems

Scheytt, J.C.; Hanke, G.; Langmann, U.;

Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 12 , Dec. 1999

Pages:1935 - 1943

[\[Abstract\]](#) [\[PDF Full-Text \(612 KB\)\]](#) [IEEE JNL](#)

20 A single-chip universal cable set-top box/modem transceiver

D'Luna, L.J.; Tan, L.K.; Mueller, D.; Laskowski, J.L.; Cameron, K.; Jind-Yeh Lee; Gee, D.; Monroe, J.S.; Law, H.S.; Chang, J.; Wakayama, M.H.; Kwan, T.; Chi-Hung Lin; Buchwald, A.; Kaylani, T.; Lu, F.; Spieker, T.; Hawley, R.; Smauli, H.;

Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999

Pages:1647 - 1660

[\[Abstract\]](#) [\[PDF Full-Text \(704 KB\)\]](#) [IEEE JNL](#)

21 Introduction to RF simulation and its application

Kundert, K.S.;

Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 9 , Sept. 1999

Pages:1298 - 1319

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) [IEEE JNL](#)

22 VHDL modeling and model testing for DSP applications

Armstrong, J.R.; Gray, F.G.; Meng-Wei Lin;

Industrial Electronics, IEEE Transactions on , Volume: 46 , Issue: 1 , Feb. 1999

Pages:13 - 22

[\[Abstract\]](#) [\[PDF Full-Text \(592 KB\)\]](#) [IEEE JNL](#)

23 A fast-search motion estimation method and its VLSI architecture

Pei-Yin Chen; Jet Min Jou;

Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 9 , Sept. 1999

Pages:1233 - 1240

[\[Abstract\]](#) [\[PDF Full-Text \(580 KB\)\]](#) [IEEE JNL](#)

24 Subject Index

Circuits and Systems II: Analog and Digital Signal Processing, IEEE

Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Volume: 46 , Issue: 12 , Dec. 1999
Pages:7 - 26

[\[Abstract\]](#) [\[PDF Full-Text \(284 KB\)\]](#) IEEE JNL

25 IEEE standard for integrated circuit (IC) delay and power calculation system

IEEE Std 1481-1999 , 26 June 1999
Pages:i - 390

[\[Abstract\]](#) [\[PDF Full-Text \(1780 KB\)\]](#) IEEE STD

26 C-based SoC design flow and EDA tools: an ASIC and system vendor perspective

Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1507 - 1522

[\[Abstract\]](#) [\[PDF Full-Text \(388 KB\)\]](#) IEEE JNL

27 An industrial view of electronic design automation

MacMillen, D.; Camposano, R.; Hill, D.; Williams, T.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1428 - 1448

[\[Abstract\]](#) [\[PDF Full-Text \(180 KB\)\]](#) IEEE JNL

28 Designing electronic engines with electronic engines: 40 years of bootstrapping of a technology upon itself

Jess, J.A.G.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 19 , Issue: 12 , Dec. 2000
Pages:1404 - 1427

[\[Abstract\]](#) [\[PDF Full-Text \(280 KB\)\]](#) IEEE JNL

29 Computer-aided design of analog and mixed-signal integrated circuits

Gielen, G.G.E.; Rutenbar, R.A.;
Proceedings of the IEEE , Volume: 88 , Issue: 12 , Dec. 2000
Pages:1825 - 1854

[\[Abstract\]](#) [\[PDF Full-Text \(552 KB\)\]](#) IEEE JNL

30 IP protection of DSP algorithms for system on chip implementation

Chapman, R.; Durrani, T.S.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 48 , Issue: 3 , March 2000
Pages:854 - 861

[\[Abstract\]](#) [\[PDF Full-Text \(176 KB\)\]](#) IEEE JNL

31 A microprocessor design project in an introductory VLSI course

Brown, R.B.; Lomax, R.J.; Carichner, G.; Drake, A.J.;

Education, IEEE Transactions on , Volume: 43 , Issue: 3 , Aug. 2000

Pages:353 - 361

[\[Abstract\]](#) [\[PDF Full-Text \(524 KB\)\]](#) IEEE JNL

32 PROTEUS-Lite project: dedicated to developing a telecommunication-oriented FPGA and its applications

Miyazaki, T.; Takahara, A.; Murooka, T.; Katayama, M.; Ichimori, T.;

Shirakawa, K.; Tsutsui, A.; Fukami, K.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 8 , Issue: 4 , Aug. 2000

Pages:401 - 414

[\[Abstract\]](#) [\[PDF Full-Text \(632 KB\)\]](#) IEEE JNL

33 A 30-frames/s megapixel real-time CMOS image processor

Doswald, D.; Hafliger, J.; Blessing, P.; Felber, N.; Niederer, P.; Fichtner, W.;

Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 11 , Nov. 2000

Pages:1732 - 1743

[\[Abstract\]](#) [\[PDF Full-Text \(320 KB\)\]](#) IEEE JNL

34 System design consideration for digital wheelchair controller

Ruei-Xi Chen; Liang-Gee Chen; Lilin Chen;

Industrial Electronics, IEEE Transactions on , Volume: 47 , Issue: 4 , Aug. 2000

Pages:898 - 907

[\[Abstract\]](#) [\[PDF Full-Text \(1496 KB\)\]](#) IEEE JNL

35 Rapid prototyping using field-programmable logic devices

Hamblen, J.O.;

Micro, IEEE , Volume: 20 , Issue: 3 , May-June 2000

Pages:29 - 37

[\[Abstract\]](#) [\[PDF Full-Text \(1536 KB\)\]](#) IEEE JNL

36 A new qualitative metric for assessing advanced graduate courses in computer engineering and science

Ghosh, S.;

Circuits and Devices Magazine, IEEE , Volume: 16 , Issue: 6 , Nov. 2000

Pages:11 - 20

[\[Abstract\]](#) [\[PDF Full-Text \(204 KB\)\]](#) IEEE JNL

37 Limitations and challenges of computer-aided design technology for CMOS VLSI

Bryant, R.E.; Kwang-Ting Cheng; Kahng, A.B.; Keutzer, K.; Maly, W.; Newton, R.;

Pileggi, L.; Rabaey, J.M.; Sangiovanni-Vincentelli, A.;

Proceedings of the IEEE , Volume: 89 , Issue: 3 , March 2001

Pages:341 - 365

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) IEEE JNL

38 Quantitative study of the impact of design and synthesis options on processor core performance

Bautista, T.; Nunez, A.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 3 , June 2001

Pages:461 - 473

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) IEEE JNL

39 An efficient architecture for two-dimensional discrete wavelet transform

Po-Cheng Wu; Liang-Gee Chen;

Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 11 , Issue: 4 , April 2001

Pages:536 - 545

[\[Abstract\]](#) [\[PDF Full-Text \(644 KB\)\]](#) IEEE JNL

40 Activity-driven clock design

Farrahi, A.H.; Chunhong Chen; Srivastava, A.; Tellez, G.; Sarrafzadeh, M.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 , Issue: 6 , June 2001

Pages:705 - 714

[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#) IEEE JNL

41 A new contactless smart card IC using an on-chip antenna and an asynchronous microcontroller

Abrial, A.; Bouvier, J.; Renaudin, M.; Senn, P.; Vivet, P.;

Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 7 , July 2001

Pages:1101 - 1107

[\[Abstract\]](#) [\[PDF Full-Text \(128 KB\)\]](#) IEEE JNL

42 80-Mb/s QPSK and 72-Mb/s 64-QAM flexible and scalable digital OFDM transceiver ASICs for wireless local area networks in the 5-GHz band

Eberle, W.; Derudder, V.; Vanwijnsberghe, G.; Vergara, M.; Deneire, L.; Van der Perre, L.; Engels, M.G.E.; Bolsens, I.; De Man, H.;

Solid-State Circuits, IEEE Journal of , Volume: 36 , Issue: 11 , Nov. 2001

Pages:1829 - 1838

[\[Abstract\]](#) [\[PDF Full-Text \(333 KB\)\]](#) IEEE JNL

43 Software implementation of synchronous programs

Andre, C.; Boulanger, F.; Girault, A.;

Application of Concurrency to System Design, 2001. Proceedings. 2001 International Conference on , 25-29 June 2001

Pages:133 - 142

[\[Abstract\]](#) [\[PDF Full-Text \(238 KB\)\]](#) IEEE CNF

44 IEEE standard Verilog hardware description language

IEEE Std 1364-2001 , 2001
Pages:0_1 - 856

[\[Abstract\]](#) [\[PDF Full-Text \(3773 KB\)\]](#) IEEE STD

45 Chip design of portable speech memopad suitable for persons with visual disabilities

Jhing-Fa Wang; Jia-Ching Wang; Han-Chiang Chen; Tai-Lung Chen; Chin-Chan Chang; Ming-Chi Shih;

Speech and Audio Processing, IEEE Transactions on , Volume: 10 , Issue: 8 , Nov. 2002

Pages:644 - 658

[\[Abstract\]](#) [\[PDF Full-Text \(1226 KB\)\]](#) IEEE JNL

46 A "flying-adder" architecture of frequency and phase synthesis with scalability

Liming Xiu; Zhihong You;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 5 , Oct. 2002

Pages:637 - 649

[\[Abstract\]](#) [\[PDF Full-Text \(680 KB\)\]](#) IEEE JNL

47 FPGA realization of wavelet transform for detection of electric power system disturbances

Shyh-Jier Huang; Tsai-Ming Yang; Jiann-Tseng Huang;

Power Delivery, IEEE Transactions on , Volume: 17 , Issue: 2 , April 2002

Pages:388 - 394

[\[Abstract\]](#) [\[PDF Full-Text \(346 KB\)\]](#) IEEE JNL

48 An introductory digital design course using a low-cost autonomous robot

Newman, K.E.; Hamblen, J.O.; Hall, T.S.;

Education, IEEE Transactions on , Volume: 45 , Issue: 3 , Aug. 2002

Pages:289 - 296

[\[Abstract\]](#) [\[PDF Full-Text \(308 KB\)\]](#) IEEE JNL

49 Performance characterization of FPGA techniques for calibration and beamforming in smart antenna applications

Nuteson, T.W.; Stocker, J.E.; Clark, J.S.; Haque, D.S.; Mitchell, G.S.;

Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 12 , Dec. 2002

Pages:3043 - 3051

[\[Abstract\]](#) [\[PDF Full-Text \(859 KB\)\]](#) IEEE JNL

50 Minimizing memory access energy in embedded systems by selective instruction compression

Benini, L.; Macii, A.; Macii, E.; Poncino, M.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 , Issue: 5 , Oct. 2002

Pages:521 - 531

[\[Abstract\]](#) [\[PDF Full-Text \(793 KB\)\]](#) **IEEE JNL**

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1 Hardware implementation of a multiprocessor system controlled by Petri nets

Anzai, F.; Kawahara, N.; Takei, T.; Watanabe, T.; Murakoshi, H.; Kondo, T.; Dohi, Y.;

Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on , 15-19 Nov. 1993
 Pages:121 - 126 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) **IEEE CNF**

2 A synthesis method for mixed synchronous/asynchronous behavior

Tsung-Yi Wu; Tzu-Chie Tien; Wu, A.C.-H.; Youn-Long Lin;

European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb.-3 March 1994
 Pages:277 - 281

[\[Abstract\]](#) [\[PDF Full-Text \(436 KB\)\]](#) **IEEE CNF**

3 Autocircuit: a clock edge general behavioral synthesis system with a direct path to physical datapaths

Ugurdag, H.F.; Fuhrman, T.E.;

Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE International Conference on , 7-9 Oct. 1996
 Pages:514 - 523

[\[Abstract\]](#) [\[PDF Full-Text \(1072 KB\)\]](#) **IEEE CNF**

4 Precision and performance of numerically controlled oscillators with hybrid function generators

Janiszewski, I.; Hoppe, B.; Meuth, H.;

Frequency Control Symposium and PDA Exhibition, 2001. Proceedings of the

2001 IEEE International , 6-8 June 2001
Pages:744 - 752

[\[Abstract\]](#) [\[PDF Full-Text \(768 KB\)\]](#) **IEEE CNF**

5 Numerically controlled oscillators with hybrid function generators

Janiszewski, I.; Hoppe, B.; Meuth, H.;

Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on
, Volume: 49 , Issue: 7 , July 2002

Pages:995 - 1004

[\[Abstract\]](#) [\[PDF Full-Text \(1097 KB\)\]](#) **IEEE JNL**

6 HDL synthesis and simulation of eight bit DSP based micro-controller for image processing applications

Rangarajan, P.; Kutraleeshwaran, V.; Vaasanthy, K.; Perinbam, R.P.;

Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on , Volume: 3 , 4-7 Aug. 2002

Pages:III - 609-12 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(282 KB\)\]](#) **IEEE CNF**

7 Low cost floating point arithmetic unit design

Seungchul Kim; Yongjoo Lee; Wookyeong Jeong; Yongsurk Lee;

ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on , 6-8 Aug. 2002

Pages:217 - 220

[\[Abstract\]](#) [\[PDF Full-Text \(330 KB\)\]](#) **IEEE CNF**

8 A low-cost digital controller for a switching DC converter with improved voltage regulation

Islam, M.M.; Allee, D.R.; Konasani, S.; Rodriguez, A.A.;

Power Electronics Letters, IEEE , Volume: 2 , Issue: 4 , Dec. 2004

Pages:121 - 124

[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#) **IEEE JNL**

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